<table>
<thead>
<tr>
<th><strong>Module Code</strong></th>
<th>CS2022</th>
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<tbody>
<tr>
<td><strong>Module Title</strong></td>
<td>Computer Architecture II</td>
</tr>
<tr>
<td><strong>Pre-requisites</strong></td>
<td>None</td>
</tr>
<tr>
<td><strong>ECTS</strong></td>
<td>5</td>
</tr>
<tr>
<td><strong>Chief Examiner</strong></td>
<td>Dr Michael Manzke</td>
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<tr>
<td><strong>Teaching Staff</strong></td>
<td>Dr Michael Manzke</td>
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<tr>
<th><strong>Contact Hours</strong></th>
<th><strong>Lecture hours</strong></th>
<th><strong>Lab hours</strong></th>
<th><strong>Tutorial hours</strong></th>
<th><strong>Total</strong></th>
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<tr>
<td></td>
<td>22</td>
<td>33(11 each)</td>
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<td>33</td>
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**Comments:** Attendance at all lectures, labs and tutorials is compulsory.

**Aims**

The lectures and tutorials treat the detailed design and organisation of microprocessor.

Course Work: Two projects using VHDL and ModelSim to simulate and test their design.

1. A processor unit (ALU + shifter + fast registers) design and simulation,
2. An instruction processor design and simulation.

Contents: Digital Logic, Register transfer definition, micro-operations, bus transfers, ALU design, shifter design, hardwired control design, microprogrammed processor control, design of an instruction processor.

The aims of the course are to learn register-transfer specification and design and learn the fundamentals of an instruction processor.

**Learning Outcomes**

Students will be able to

- design substantial logic circuits using register transfer descriptions;
- test and verify their design using an industry standard hardware description language (VHDL);
- understand the organisation and execution behaviour of general-
### Syllabus
Specific topics addressed in this module include:
- Digital Logic
- Register transfer language
- ALU and shifter design
- Multiplexer and tristate busses.
- Datapath design
- Instruction fetch-decode-execute cycle

### Assessment
Assessment is by examination (80%) and continuous assessment (20%).
Continuous assessment is composed of a number of marked laboratory exercises and two substantial assignments.
Assessment in supplemental examinations is by 100% exam.

### Bibliography
Recommended text:
- Introductory VHDL: From Simulation to Synthesis
- Logic and Computer Design Fundamentals” 2nd Edition updated, Mano

Additional recommended texts:

### Website