



# SCI Basics

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## What is SCI



- The SCI standard ANSI/IEEE 1596-1992 defines a point-to-point interface and a set of packet protocols.
- The SCI protocols use small packet sizes with a 16-byte header and data sizes of 16, 64, (128) and {256} bytes. Each packet is protected by a 16-bit CRC code. An SCI interface has two unidirectional links that operate concurrently.
- The SCI protocols support shared memory by encapsulating bus requests and responses into SCI request and response packets. Packet-based handshake protocols guarantee reliable data delivery.
- SCI use 64 bits addressing and the most significant 16 bits are used for addressing up to 64K nodes.
- A set of cache coherence protocols are defined to maintain cache coherence in a shared memory system.
- Message passing is supported by a compatible subset of the SCI protocols. This protocol subset does not invoke SCI cache coherency protocols.

### **GaAs NodeChip**

- Dolphins first realization of SCI, 1993
- 500 MB/s Link Speed
- Technology Licensed to Convex/Vitesse

### **CMOS NodeChip**

- Low Cost version, 1993
- 125 MB/s Link Speed

### **LC1**

- Available since 1995
- 200 MB/s Link Speed

### **LC2**

- Available since 1996
- 500 MB/s Link Speed

### **LC3**

- Prototype in May 2000, Volumes in August 2000





## LC3 Overview



- ANSI/IEEE Std 1596-1992 Compliant
  - LVDS Link Interface
- ANSI/IEEE Std 1159.1 JTAG support
- 272 Plastic BGA, Max 2 Watt
- Worst case timing 166MHz. Tested at 250Mhz
- 16 Internal buffers (8 Input / 8 Output )
- Virtual channels enables in order SCI packet delivery
- Two wire serial line interface for configuration and management
- Hardware Initialization
  - Automatic scrubber selection
  - Initial nodeid assignment
- Performance Counters
  - Will count packets received, bypassed, transmitted, etc.
  - Masked compare of command symbol



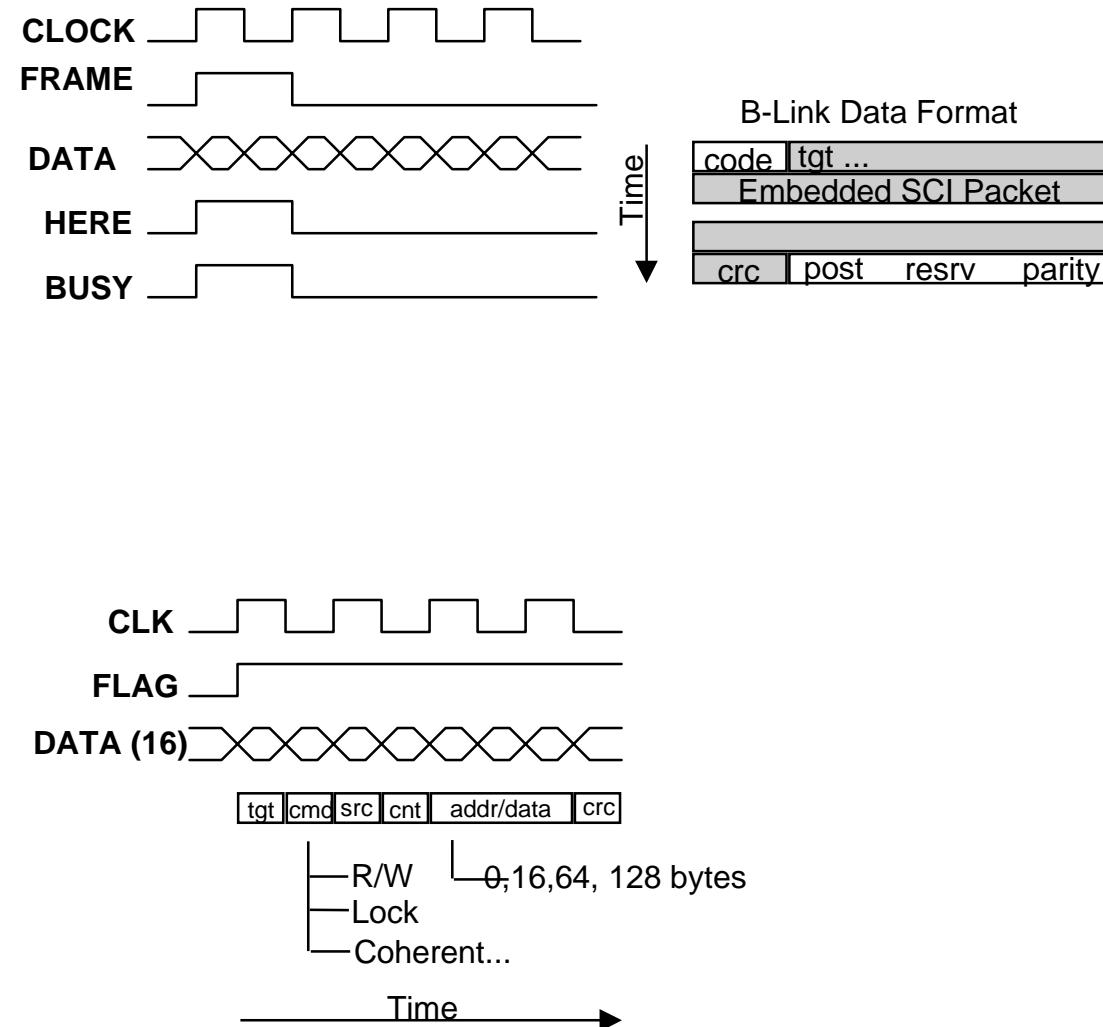
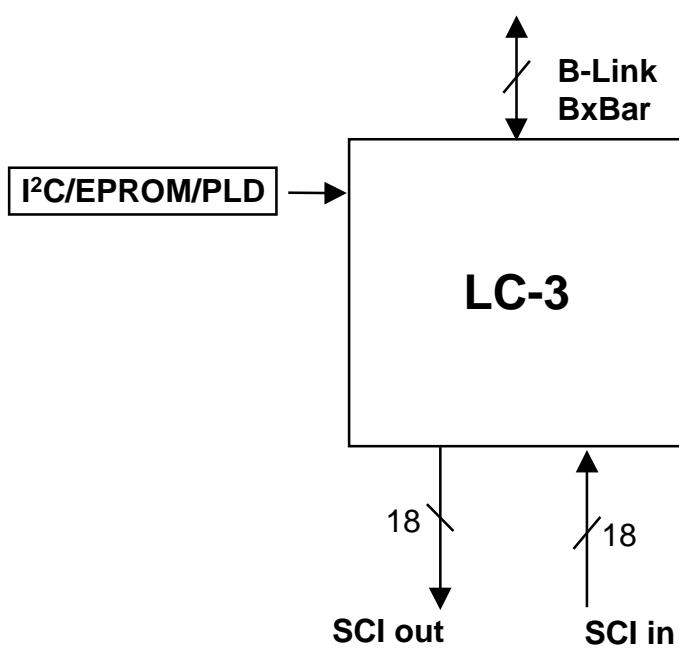
## Overview (cont.)



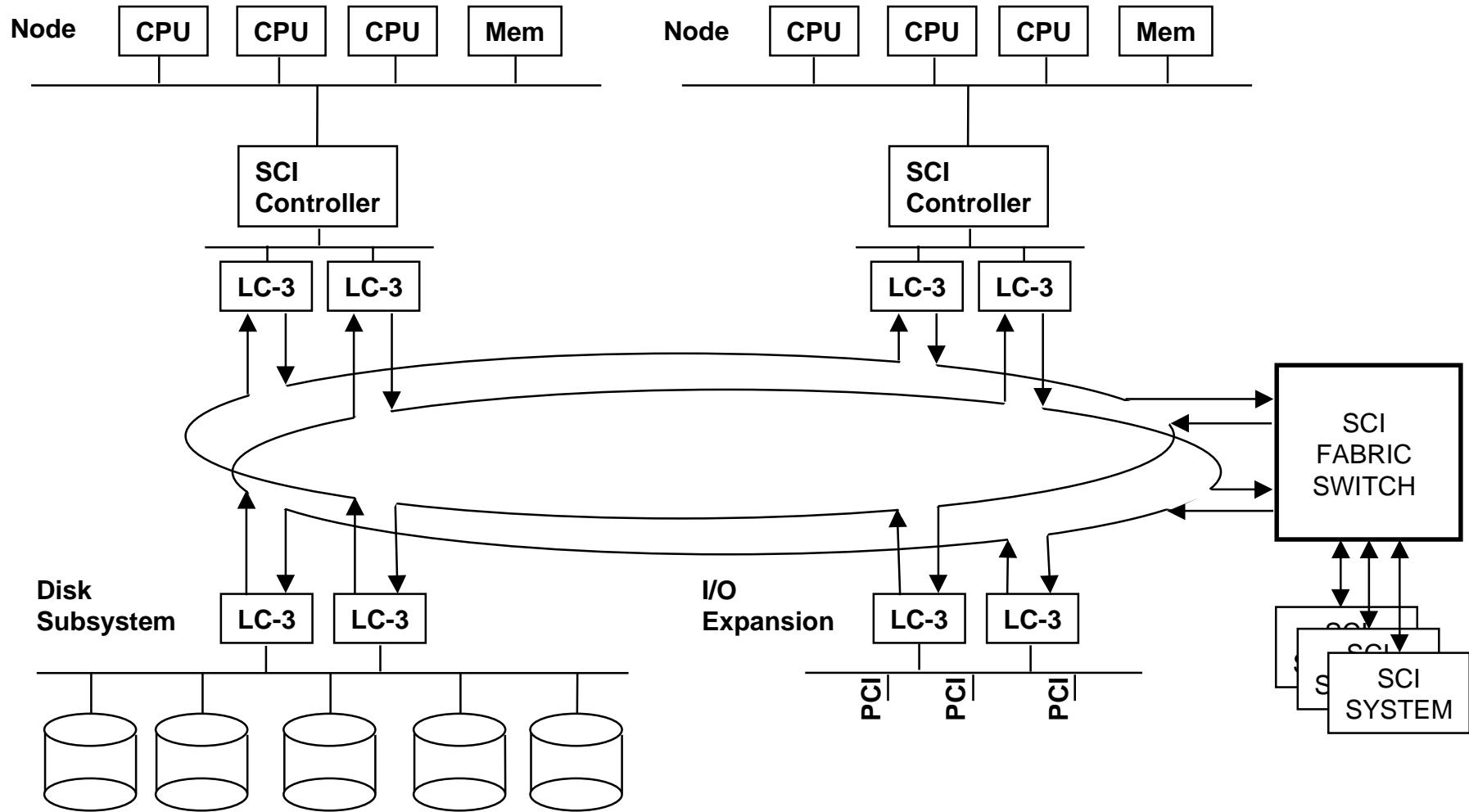
- B-Link™ and BxBar™ CrossBar interface
  - Low Signal Count
  - Embedded SCI Packets (multiplexed address/data)
  - High Performance
  - Compliant with SCI
  - Enables Pipelining (multiple outstanding transactions)
  - B-Link 100 MHz, 64 bit Shared bus
  - BxBar 100 MHz, 2x32 Bit Crossbar Interface



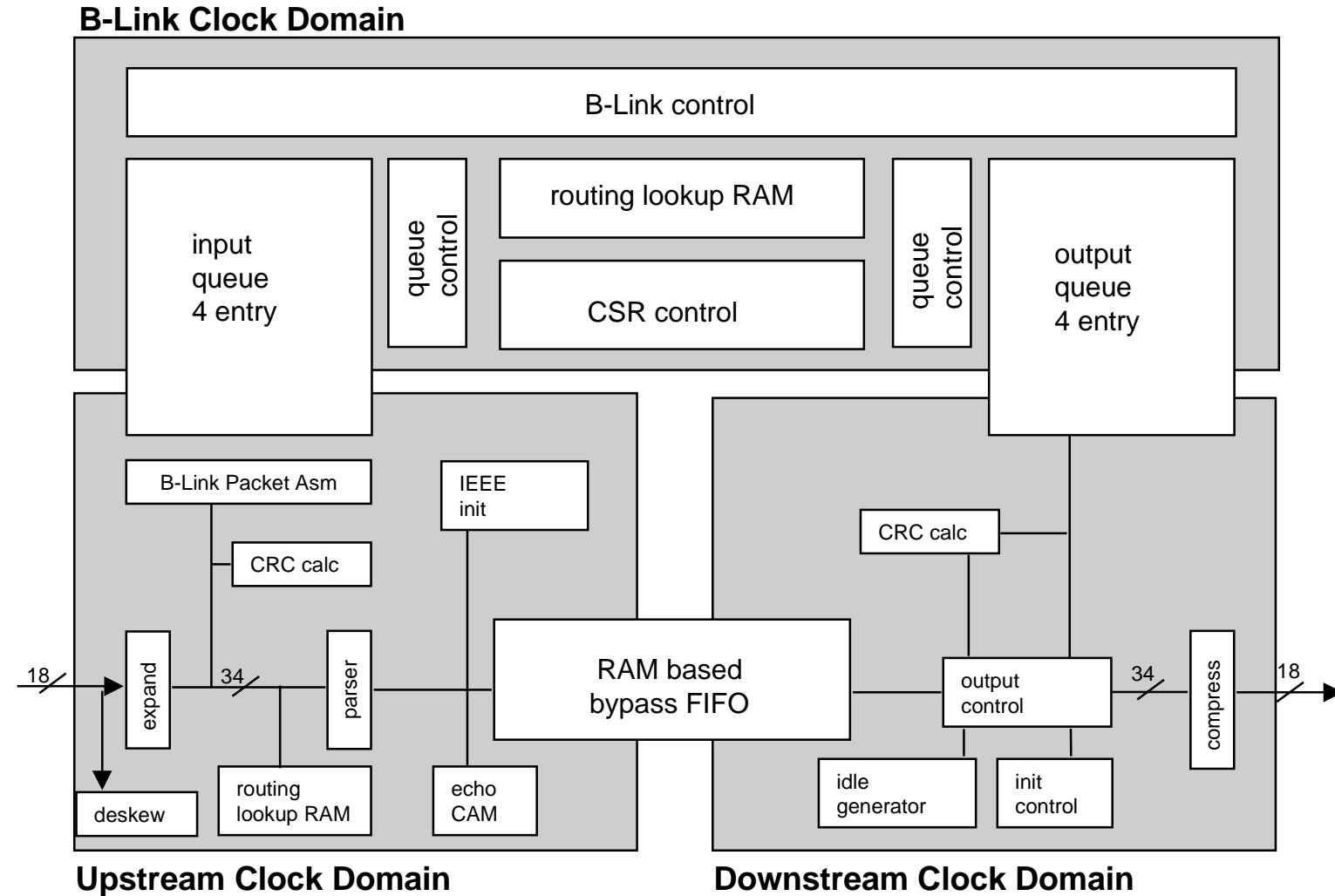
## LinkController-3 Overview



## LC-3 APPLICATION EXAMPLE



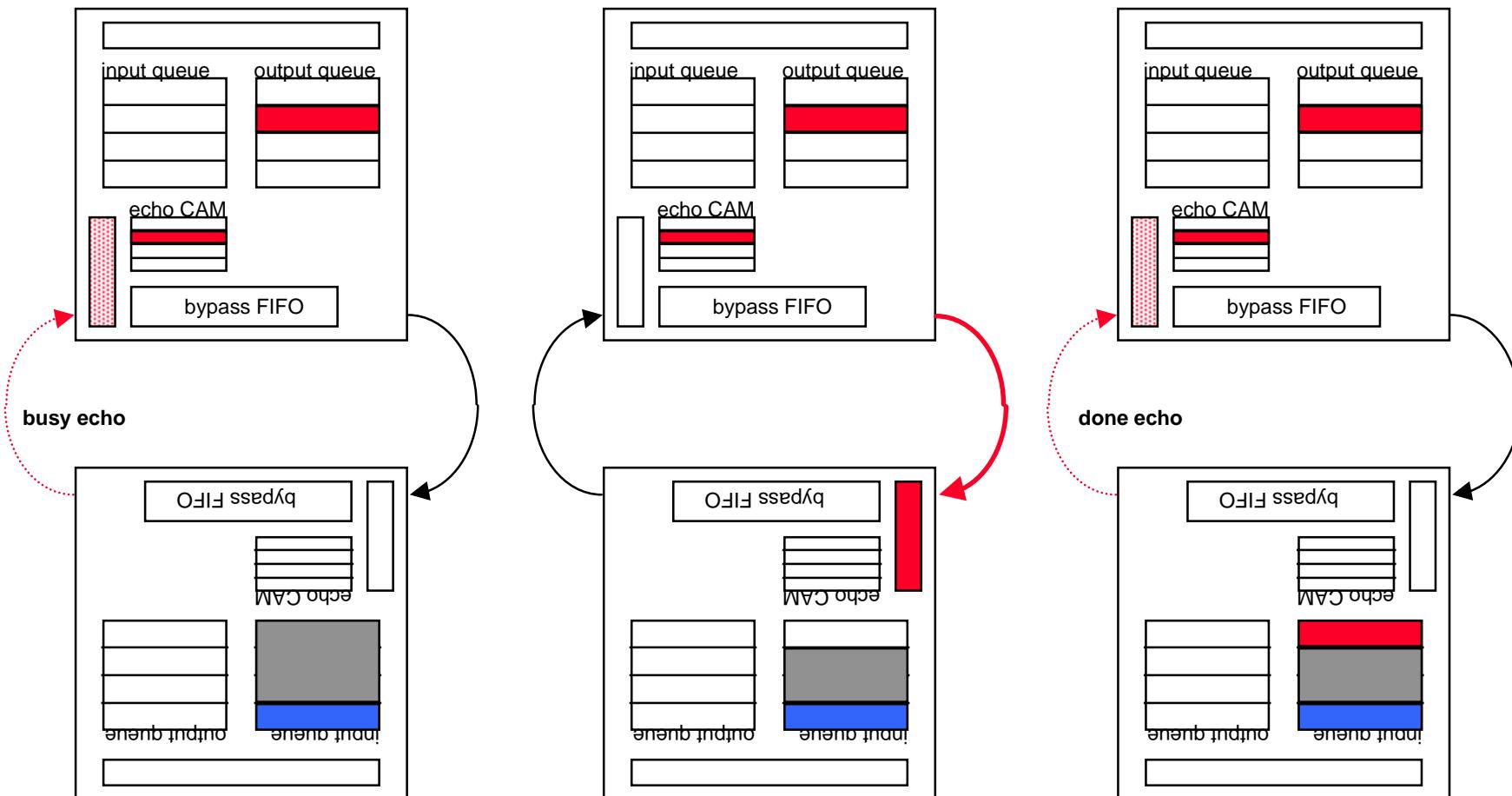
# LC Simplified Block Diagram



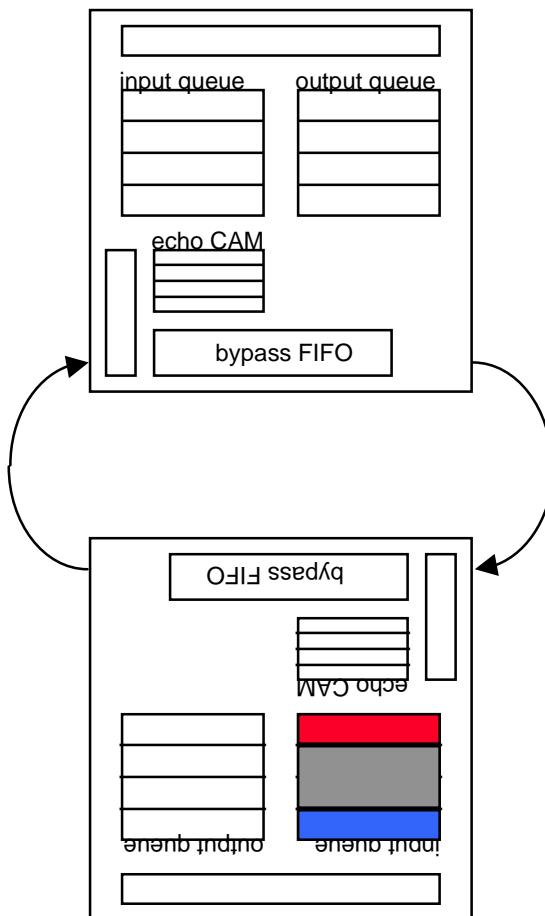
## Sample Packet Traversal



## Sample Packet Traversal (cont.)



## Sample Packet Traversal (cont.)





## ❑ 64 bit / 66 MHz PCI Bridge

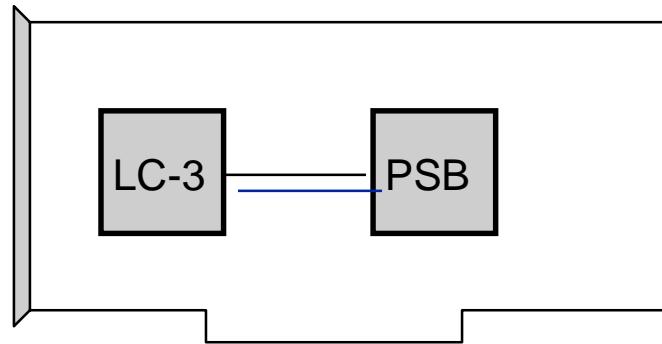
- 313 BGA - Power consumption : 3 Watt
- PCI 2.1 Compliant
- Smart Chained DMA
  - ◆ DMA barrier operation
  - ◆ Complete or stop
- Performance enhancements
  - ◆ > 300 MB/s
  - ◆ 128 Byte SCI packets ( short 256 )
  - ◆ Enhanced Internal Logic
- Samples available now
- Volumes from December 2000



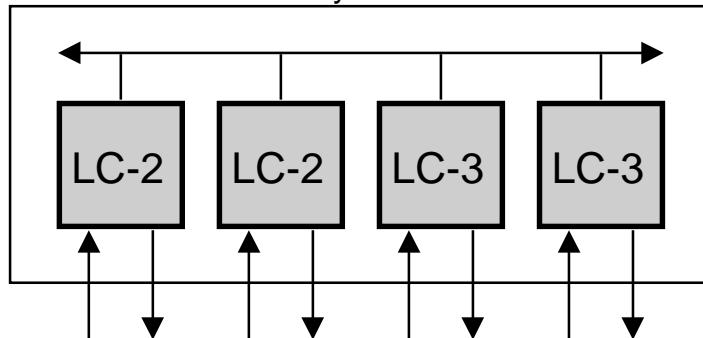
## Application Examples



PCI-SCI Adapter card



Low Cost  
4-way Switch



High Performance  
8-way Scalable Switch

