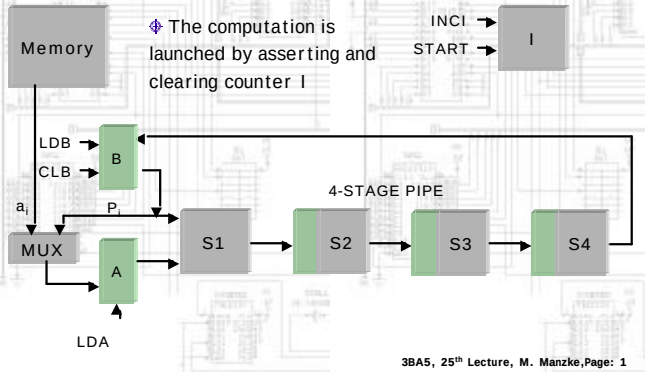
## Schematic






## Reservation Table + Control Signals

| CLK | 0 | 1 | 2 | 3 | 4 | 5 | 6 | ... | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $S_1$ | | - | - | - | $P_1$ | $P_2$ | $P_3$ | .. | $P_{13}$ | $P_{14}$ | $P_{15}$ | $P_{16}$ | - | $P_{17}$ | - | $P_{18}$ | - | - | - | $P_{19}$ |
| $S_2$ | | - | - | $P_1$ | $P_2$ | $P_3$ | $P_4$ | .. | $P_{14}$ | $P_{15}$ | $P_{16}$ | - | $P_{17}$ | - | $P_{18}$ | - | - | - | $P_{19}$ | |
| $S_3$ | | - | $P_1$ | $P_2$ | $P_3$ | $P_4$ | $P_5$ | .. | $P_{15}$ | $P_{16}$ | - | $P_{17}$ | - | $P_{18}$ | - | - | - | $P_{19}$ | | |
| $S_4$ | | $P_1$ | $P_2$ | $P_3$ | $P_4$ | $P_5$ | $P_6$ | .. | $P_{16}$ | - | $P_{17}$ | - | $P_{18}$ | - | - | - | $P_{19}$ | | | |
| A | | $a_1$ | $a_2$ | $a_3$ | $a_4$ | $a_5$ | $a_6$ | .. | $a_{16}$ | - | $P_{13}$ | - | $P_{15}$ | - | - | - | $P_{17}$ | | | |
| B | 0 | 0 | 0 | 0 | 0 | $P_1$ | $P_2$ | .. | $P_{12}$ | $P_{13}$ | $P_{14}$ | $P_{15}$ | $P_{16}$ | - | $P_{17}$ | $P_{17}$ | $P_{18}$ | | | |
| | 0 | 0 | 1 | 2 | 3 | 4 | 5 | .. | 15 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| SRC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | .. | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | x | x | x | |
| LDA | 1 | 1 | 1 | 1 | 1 | 1 | 1 | .. | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| LDB | 0 | 0 | 0 | 0 | 0 | 1 | 1 | .. | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| CLB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | .. | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| START | 1 | 0 | 0 | 0 | 0 | 0 | 0 | .. | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | 1 | 2 | 3 | 4 | 5 | 6 | .. | n | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |



## Problem 3.1 - Solution

We can design a control unit for this by using a D-flip flop register whose outputs:

- AV, BV, S1V, S2V, S3V S4V

show whether the outputs of the respective registers on stages are valid.

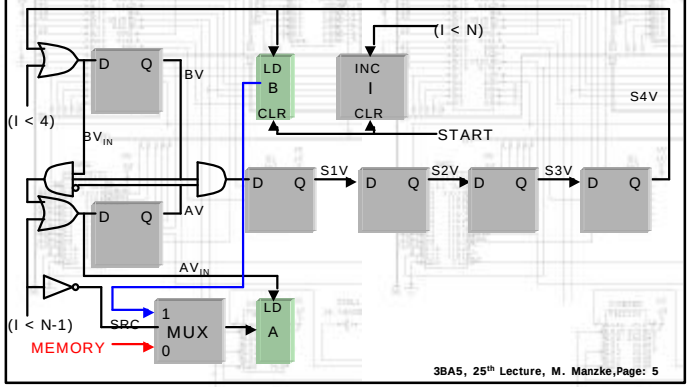


## Problem 3.1 - Solution

From these we obtain the D-flop input and control equations:

- $S1V_{IN} = AV \bullet BV$
- $S2V_{IN} = S1V$
- $S3V_{IN} = S2V$
- $S4V_{IN} = S3V$
- $AV_{IN} = I < (n-1) + BV_{IN} \bullet BV \bullet AV$
- $BV_{IN} = I < 4 + S4V$
- $LDA = AV_{IN}$
- $LDB = S4V_{IN}$
- $CLB = \overline{START}$
- $SRC = I < (N-1)$
- $CLRI = START$
- $INCI = I < N$

## Control Unit






## Problem 3.1 - Solution

- If the clock period is T and the time to add 16 numbers is T16 then
  - $T_{16} = (16 + 11) * T$
  - $T_N = (N + 11) * T$
- Note that this is not the absolute minimum time.
- If we could fetch the pairs:
  - $(a_1,a_2)$ $(a_3,a_4)$ $(a_5,a_6)$ $(a_7,a_8)$
- In the ths first four cycles we reduce the $T_N$ by four.



## Problem 3.3

- Indicate the type of data hazards (RAW, WAR, and WAW) that exist between the following instructions.

| | | |
|---|---|---|
| $i_1$: | ADD $R_1, R_2, R_3$, | -- $R_1 = R_2 + R_3$ |
| $i_2$: | ADD $R_4, R_1, R_4$, | -- $R_4 = R_1 + R_4$ |
| $i_3$: | ADD $R_3, R_1, R_2$, | -- $R_3 = R_1 + R_2$ |
| $i_4$: | ADD $R_1, R_1, R_4$, | -- $R_1 = R_1 + R_4$ |



## Problem 3.3

| | | |
|---|---|---|
| $i_1$: | ADD $R_1, R_2, R_3$, | -- |
| $i_2$: | ADD $R_4, R_1, R_4$, | -- RAW on $R_1$ |
| $i_3$: | ADD $R_3, R_1, R_2$, | -- RAW on $R_1$ $(i_1)$ |
| | | -- WAR on $R_3$ $(i_1)$ |
| $i_4$: | ADD $R_1, R_1, R_4$, | -- RAW on $R_1$ $(i_1)$ |
| | | -- RAW on $R_4$ $(i_2)$ |
| | | -- WAW on $R_1$ $(i_1)$ |