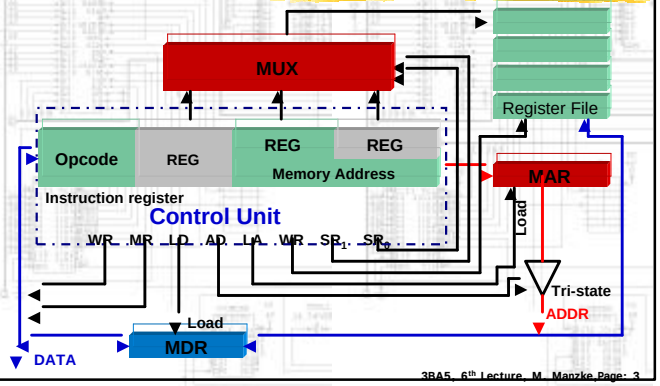
Control Unit

- Two approches:
  - Hardwired
  - Microprogram
- Single cycle datapath require:
  - Truestable -> hardwired solution
- Multicycle datapath control may be defined through:
  - Microprogramming

Control Signal from Example

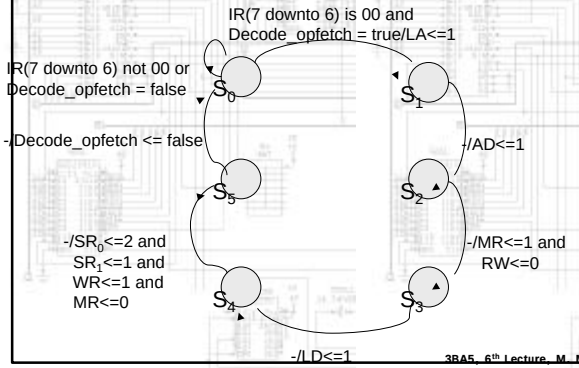
- RW
  - Perform read/write operations from/to mem
- MR
  - Enable the chip select of the mem
- LD
  - Load data from data bus to MDR
- AD
  - Load address from MAR to address bus
- LA
  - Load the right most 4 bits of IR to MAR
- WR
  - Perform read/write operation from register file
- SR_0 and SR_1
  - Select two bits of the IR as the address of the register file

Control Unit Example



State Diagram

This state machine may be implemented in a Programmeble Logic Array (PLA)



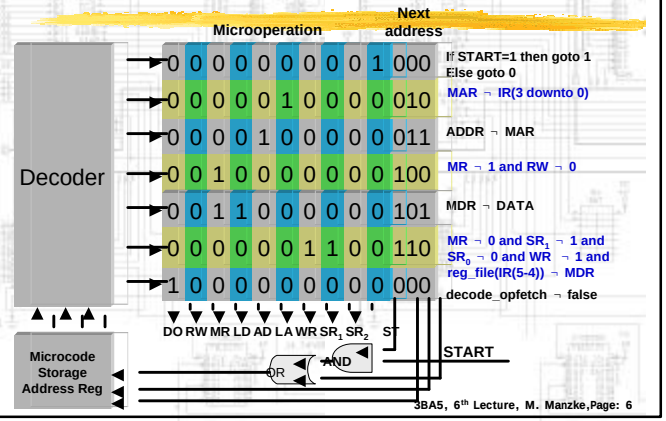
Microprogrammed

If a hardwired solution becomes to complex microprogramming may be used.

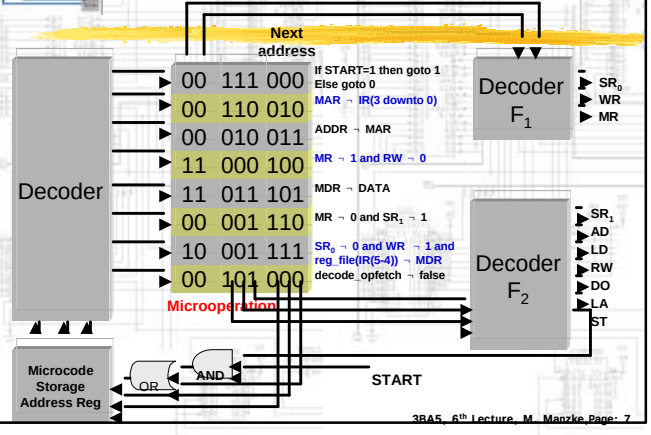
Wilkes invented this idea in 1951.

Today microprogramming is less important

Horizontal Microprogram



Vertical Microprogram

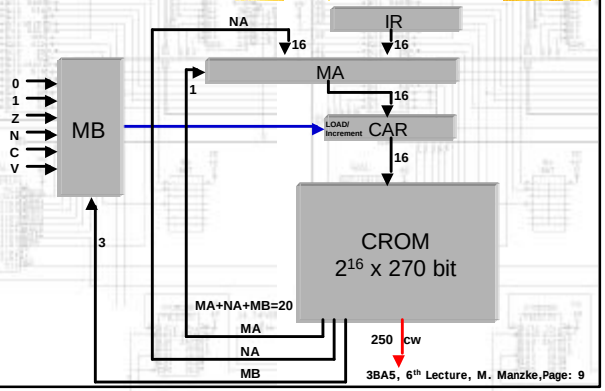


Split-level control memory

Another approach

- When a typical instruction set is microcoded:
  - Few different control words (cw) are found
  - Which results in an inefficient use of the CROM
- Consider a 64K CROM delivering 250-bit cw
  - See next page:

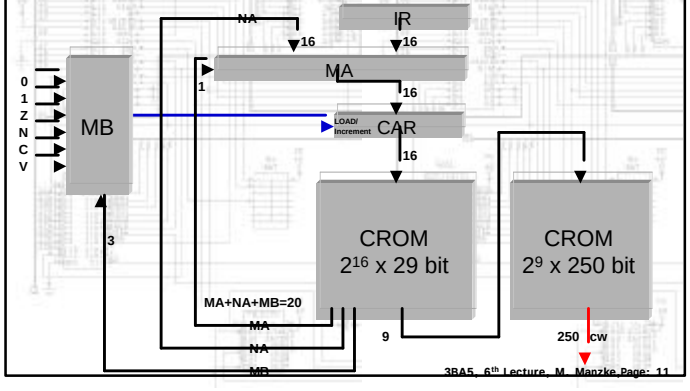
Single–level Control Store



512 Different CWs

- If, however, in the CROM we find only 512 = 2^9 different CWs
  - We may re-structure it to reduce the size of the CROM

Two–level Control Store



Compare ROMs

Single-level = 2^{16}x270 = 2160 Kbytes

Two-level = 2^{16}x29 + 2^9x250

= 237568 bytes + 16000 bytes

= 247.625 Kbytes

Nearly one order of magnitude reduction.

Intel Pentium Pro

Example

- RISC (MIPS) architectures and CISC (Intel 80486, Pentium and Pentium Pro …) use piplining to achieve throughputs close to one instruction per clockcycle.
- But the challenges to design the control have not changed.

Control units for complex architectures

- The 80X86 instruction set contains instructions that require 10 to 100 times more cycle to execute than a MIPS instruction.
- Large number and complexity of addressing modes make the implementation of simple RISC like instruction difficulte.
- A multicycle datapath allows the design to adapt to the wide range of instruction complexity in CISC architectures.

Conclusions

- Control is determined by:
  - Instruction Set Architecture (ISA)
  - Organisation
  - Datapath design
- Single cycle organisation:
  - Control defines how control signals are set
- Multicycle organisation requires:
  - Decomposition into cycles
- The control specification must be mapped into hardware.

More Conclusions

- Control can be designed from several definitions
- There is no dependency between the choice of sequential control (state machine) and the implementation
- The implementaion depends on:
  - Size
  - Underlying technology
  - Available CAD tools

Reading

Students should revise material covered in 2BA4 by reading Chapter 5 “The Processor: Datapath and Control” in " Computer Organisation and Design", John L. Hennessy & David A. Patterson, 500.164 N85. Appendix C “Mapping Control to Hardware” in the same textbook provides information that complements ideals presented in the 3ba5 lecture.