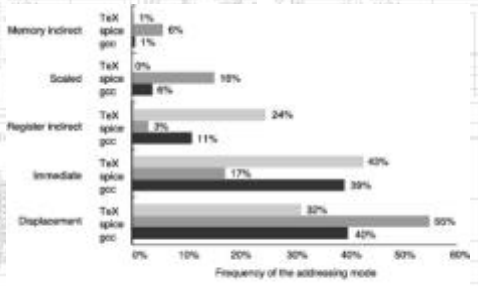
VAX Frequency of Addressing Modes

Figure 2.7 - Hennessy & Patterson



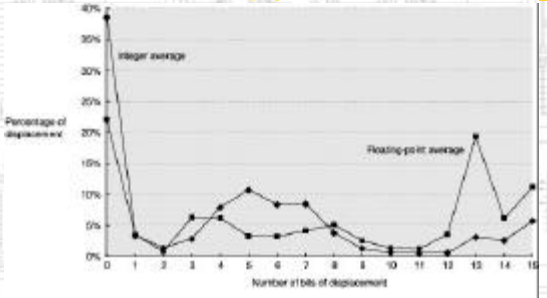
Displacement Addressing Mode

Regs[R4] <- Regs[R4] + Mem[100+Regs[R1]]

- Size of the Instruction's displacement field?
- Affects the instruction length
- The following slide shows measurements taken on a load and store architecture (Alpha) while executing a benchmark program (SPEC CPU 2000).

Displacement Value Distribution

Figure 2.8 - Hennessy & Patterson



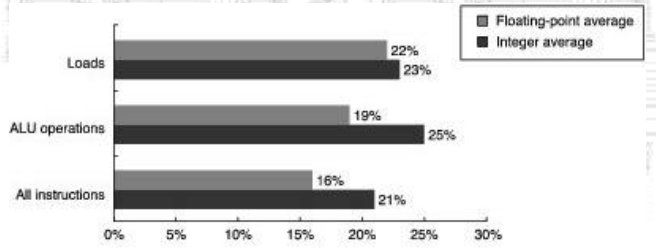
Immediate or Literal Addressing Mode

Regs[R4] <- Regs[R4] + 3

- Size of the Immediate value.
- Affects the instruction length
  - Constants mostly small
  - Addresses tend to be large.
- The following two slides shows measurements taken on a load and store architecture (Alpha) while executing a benchmark program (SPEC CPU 200).

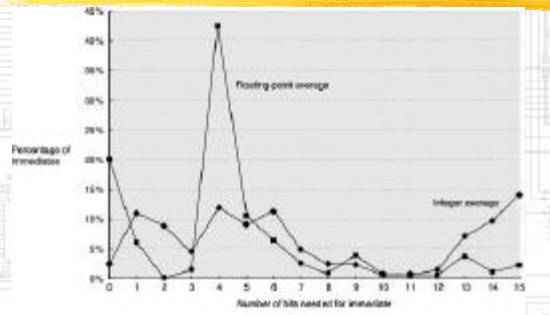
Data Transfer and ALU operations

Figure 2.9 -Hennessy & Patterson



Distribution of Immediate Values

Figure 2.10 - Hennessy & Patterson



Digital Signal Processing (DSP)

- Most DSPs provide two special addressing modes:
  - An addressing modes that simplifies the implementation of circular buffers.
  - Because DSPs deal with continuous streams of data.
  - Pointers must be incremented and reset.
  - Recent DSPs have modulo or circular addressing modes to simplify the implementation of these buffers.

Fast Fourier Transform (FFT) & DSP

- FFTs start and end their processing with data shuffled in a particular order.

$0(000_2)$	=>	$0(000_2)$
$1(001_2)$	=>	$4(100_2)$
$2(010_2)$	=>	$2(010_2)$
$3(011_2)$	=>	$6(110_2)$
$4(100_2)$	=>	$1(001_2)$
$5(101_2)$	=>	$5(101_2)$
$6(110_2)$	=>	$3(011_2)$
$7(111_2)$	=>	$7(111_2)$

- FFT Instructions reverse the binary address.

Frequency of addressing modes for TI TMS320C54xDSP

Immediate		30.02%
Displacement		10.82%
Register indirect		17.42%
Direct		11.99%
Autoincrement, preincrement (increment register before using content as address)		0%
Autoincrement, postincrement (increment register after using content as address)		18.84%
Autoincrement, preincrement with 16b immediate		0.77%
Autoincrement, preincrement with circular addressing		0.08%
Autoincrement, postincrement with 16b immediate, with circular addressing		0%
Autoincrement, postincrement by contents of AR0		1.54%
Autoincrement, postincrement by contents of AR0, with circular addressing		2.15%
Autoincrement, postincrement by contents of AR0, with bit reverse addressing		0%
Autodecrement, postdecrement (decrement register after using content as address)		6.08%
Autodecrement, postdecrement with circular addressing		0.04%
Autodecrement, postdecrement by contents of AR0		0.16%
Autodecrement, postdecrement by contents of AR0, with circular addressing		0.08%
Autodecrement, postdecrement by contents of AR0, with bit reverse addressing		0%
Total		100%

Type and Size of the Operands

- Usually the type of an operand in encoded in the opcode
- The following operands are encountered in desktop machines:
  - Character 8bits
  - Half word 16 bits
  - Word 32 bits
  - Single-precision floating point (word)
  - Double-perdition floating point (two words)
    - Floating points are mostly IEEE standard and will be discussed
  - Some ISA provide for binary-coded decimals (4bit)
- The following slide shows memory references that classify the types of data being accessed.

Distribution of Data Accesses by Size

Figure 2.12 - Hennessy & Patterson